WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first transistor having a first conduction type first semiconductor region and a second conduction type second semiconductor region formed in the first semiconductor region, the first semiconductor region being supplied with a first prescribed potential, the second semiconductor region being supplied with a second prescribed potential; and

a potential generator circuit generating the first prescribed potential, wherein

the potential generator circuit has a first power supply terminal supplied with a first power supply potential, a second power supply terminal supplied with a second power supply potential set to a higher potential than the first power supply potential, and an output terminal outputting the first prescribed potential, and

the potential generator circuit outputs the second power supply potential as the first prescribed potential when the second power supply potential is higher than a predetermined potential, and outputs the first power supply potential as the first prescribed potential when the second power supply potential is lower than the predetermined potential.

2. A semiconductor device according to claim 1, wherein the first transistor is formed of a P channel

transistor.

3. A semiconductor device according to claim 1, wherein the predetermined potential is substantially the same as the first power supply potential.

4. The semiconductor device according to claim 1, wherein the potential generator circuit comprises:

a second transistor having a source connected to the second power supply terminal supplied with the second power supply potential, and a drain connected to the output terminal outputting the first prescribed potential;

a third transistor having source and gate connected to the first power supply terminal supplied with the first power supply potential, and a drain connected to the output terminal outputting the first prescribed potential; and

an inverter circuit having an input terminal connected to the second power supply terminal, and an output terminal connected to the gate of the second transistor.

5. A semiconductor device according to claim 4, wherein the second transistor is formed of a P channel transistor, and the third transistor is formed of an N channel transistor.

6. A semiconductor device according to claim 5, wherein a threshold of the N channel transistor is lower than a voltage in which a PN junction becomes

forward biased.

7. A semiconductor device according to claim 4, wherein when the second power supply potential is higher than the predetermined potential, the second transistor turns on, and the second power supply potential is outputted from the output terminal as the first prescribed potential, and when the second power supply potential is lower than the predetermined potential, the second transistor turns off and the third transistor turns on, and the first power supply potential is outputted from the output terminal as the first prescribed potential.

8. A semiconductor device according to claim 7, wherein the turn on and off of the second transistor is controlled by an output of the inverter circuit.

9. The semiconductor device according to claim 1, wherein the potential generator circuit comprises:

a second transistor having a source connected to the second power supply terminal supplied with the second power supply potential, and a drain connected to the output terminal outputting the first prescribed potential;

a third transistor having source and gate connected to the first power supply terminal supplied with the first power supply potential, and a drain connected to the output terminal outputting the first prescribed potential; and

a comparator circuit including a differential amplifier circuit having a pair of input terminals and an output terminal;

wherein one of said pair of input terminals of the differential amplifier circuit of the comparator circuit is connected with the second power supply terminal, the other thereof is connected with a source of a fourth transistor having drain and gate both connected to the first power supply terminal, and the output terminal of the differential amplifier circuit of the comparator circuit is connected to the gate of the second transistor.

10. A semiconductor device according to claim 9, wherein the second transistor is formed of a P channel transistor, the third transistor is formed of an N channel transistor, and the fourth transistor is formed of an N channel transistor.

11. A semiconductor device according to claim 9, wherein a threshold of the N channel transistor is lower than a voltage in which a PN junction becomes forward biased.

12. A semiconductor device according to claim 9, wherein the fourth transistor has substantially the same threshold as the third transistor.

13. The semiconductor device according to claim 9, wherein when the second power supply potential is higher than the predetermined potential, the second

transistor turns on, and the second power supply potential is outputted from the output terminal as the first prescribed potential, and when the second power supply potential is lower than the predetermined potential, the third transistor turns on while the second transistor turns off, and the first power supply potential is outputted from the output terminal as the first prescribed potential.

14. A semiconductor device according to claim 13, wherein the turn on and off of the second transistor is controlled by an output of the differential amplifier circuit of the comparator circuit.

15. A semiconductor device comprising:

a first transistor having a first conduction type first semiconductor region and a second conduction type second semiconductor region formed in the first semiconductor region, the first semiconductor region being supplied with a first prescribed potential, the second semiconductor region being supplied with a second prescribed potential; and

a potential generator circuit generating the first prescribed potential, wherein

the potential generator circuit has a first power supply terminal supplied with a first power supply potential, a second power supply terminal supplied with a second power supply potential set to a higher potential than the first power supply potential, and an

output terminal outputting the first prescribed potential, and

the potential generator circuit comprises:

a second transistor having a source connected to the second power supply terminal supplied with the second power supply potential, and a drain connected to the output terminal outputting the first prescribed potential;

a third transistor having source and gate connected to the first power supply terminal supplied with the first power supply potential, and a drain connected to the output terminal outputting the first prescribed potential; and

an inverter circuit having an input terminal connected to the second power supply terminal, and an output terminal connected to the gate of the second transistor.

16. A semiconductor device according to claim 15, wherein the first transistor is formed of a P channel transistor.

17. A semiconductor device comprising:

a first transistor having a first conduction type first semiconductor region and a second conduction type second semiconductor region formed in the first semiconductor region, the first semiconductor region being supplied with a first prescribed potential, the second semiconductor region being supplied with a

second prescribed potential; and

a potential generator circuit generating the first prescribed potential, wherein

the potential generator circuit has a first power supply terminal supplied with a first power supply potential, a second power supply terminal supplied with a second power supply potential set to a higher potential than the first power supply potential, and an output terminal outputting the first prescribed potential, and

the potential generator circuit comprises:

a second transistor having a source connected to the second power supply terminal supplied with the second power supply potential, and a drain connected to the output terminal outputting the first prescribed potential;

a third transistor having source and gate connected to the first power supply terminal supplied with the first power supply potential, and a drain connected to the output terminal outputting the first prescribed potential; and

a comparator circuit including a differential amplifier circuit having a pair of input terminals and an output terminal;

wherein one of said pair of input terminals of the differential amplifier circuit of the comparator circuit is connected with the second power supply

terminal, the other thereof is connected with a source of a fourth transistor having drain and gate both connected to the first power supply terminal, and the output terminal of the differential amplifier circuit of the comparator circuit is connected to the gate of the second transistor.

18. A semiconductor device according to claim 17, wherein the second transistor is formed of a P channel transistor, the third transistor is formed of an N channel transistor, and the fourth transistor is formed of an N channel transistor.

19. A semiconductor device according to claim 17, wherein the third transistor has a lower threshold than the second transistor.

20. A semiconductor device according to claim 17, wherein the fourth transistor has substantially the same threshold as the third transistor.